



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/891,020	06/25/2001	Gordon J. Harris	07072-137001/CS-005	9419

26161 7590 12/04/2006

FISH & RICHARDSON PC
P.O. BOX 1022
MINNEAPOLIS, MN 55440-1022

EXAMINER

NGUYEN, QUANG N

ART UNIT	PAPER NUMBER
----------	--------------

2141

DATE MAILED: 12/04/2006

Please find below and/or attached an Office communication concerning this application or proceeding.



UNITED STATES PATENT AND TRADEMARK OFFICE

Commissioner for Patents
United States Patent and Trademark Office
P.O. Box 1450
Alexandria, VA 22313-1450
www.uspto.gov

**BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES**

Application Number: 09/891,020
Filing Date: June 25, 2001
Appellant(s): HARRIS, GORDON J.

MAILED

DEC 04 2006

Technology Center 2100

Frank R. Occhiuti
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 09/06/2006 appealing from the Office action mailed 04/19/2006.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings, which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

A substantially correct copy of appealed claims 24-25 appears on page 24 of the Appendix to the appellant's brief. The minor errors are as follows:

- On line 1 of claim 24: "The method of claim 6, ..." should be "The system of claim 6, ...".
- On line 1 of claim 25: "The method of claim 14, ..." should be "The article of claim 14, ...".

(8) Evidence Relied Upon

- US Patents and US Patent Application Publication:

5,860,146	Vishin et al.	01-1999
6,374,341	Nijhawan et al.	04-2002
6,934,760	Westbrook et al.	08-2005
2003/0097481	Richter	05-2003

- Non Patent Literature:

"What is switch? - A Word Definition From the Webopedia Computer Dictionary",
<http://www.webopedia.com/TERM/s/switch.html>

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claim Objections

1. Claims 24 and 25 are objected to because of the following informalities:
 - Claim 24: "The method of claim 6" should be "The system of claim 6".
 - Claim 25: "The method of claim 14" should be "The article of claim 14".

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

3. **Claims 1-11 and 14-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nijhawan et al. (US 6,374,341), hereinafter "Nijhawan", in view of Vishin et al. (US 5,860,146), hereinafter "Vishin", and further in view of Applicant Admitted Prior Art (AAPA).**

4. As to claim 1, **Nijhawan** teaches a method comprising:

moving data into a physical memory page, wherein the physical memory page comprising a plurality of physical memory clusters (*moving data into a plurality of physical memory blocks 92 and 94 that are aligned as illustrated in Fig. 9*) (**Nijhawan, Fig. 9 and col. 10, lines 8-16**);

creating a logical page providing an aligned view of the data (*a logical page is created/mapped to a physical page as illustrated in Fig. 9*) (**Nijhawan, col. 4, lines 3-6**);

establishing a relationship between the logical page and the physical memory page such that the logical page is associated with the plurality of physical memory clusters (*a logical page number is mapped or translated to a physical page number, and the target physical location within the page can be accessed, as illustrated in Fig. 9*) (**Nijhawan, Fig. 9 and col. 4, lines 3-27**);

forwarding a list of the logical pages to a storage resource such that the data referenced by the logical pages are stored subsequently into a storage resource (*as illustrated in Fig. 8, the linear address translation maintains all memory blocks are aligned, no two such memory blocks are mapped in the same linear address, hence no overlapping mappings, i.e., stored subsequently, and the block of memory is correctly sized-aligned in physical memory as illustrated in Fig. 9*) (**Nijhawan, Figs. 8-9, col. 9, lines 26-37 and col. 10, lines 7-16**).

However, **Nijhawan** does not explicitly teach moving data from a network layer into a physical memory page, wherein the network layer receives and transmits the data as data packets that are odd sized, arrive asynchronously, and contain metadata embedded with real data.

In an analogous art, **Vishin** teaches a distributed computer system having a primary translation lookaside buffer for storing page table entries and translating virtual (*i.e., logical*) addresses into physical addresses governed by a memory controller 112 that can also send requests via a network 114 to pull in pages of data stored in the memory stores or secondary memory of other clusters 102 or other devices coupled to

the network 114 via network switches as illustrated in Figs. 1 and 9 (*Examiner respectfully submits that one of ordinary skill in the art would appreciate that in networks, network switches operate at the data link layer (layer 2) and sometimes at the network layer (layer 3) to filter and forward data packets between network segments, hence, in order to move, access, or write data from/to a remote cluster 102 connected to the network 114 via network switches to pull in pages of data stored in the memory stores or secondary memory of other clusters 102 as illustrated in Figs. 1 and 9, it should include the step of moving data from a network layer into the memory stores, i.e., moving data from network layer into a physical memory*) (**Vishin, Figs. 1 and 9, and col. 1, lines 12-24**).

Also, Applicant Admitted Prior Art (**AAPA**) teaches in an Ethernet network, network data can be transmitted and received as data packets that can be characterized as being odd-sized, arriving asynchronously or without warning, and having metadata such as protocol information embedded along with real data (**AAPA, Background, page 1, lines 8-12**).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to combine the teachings of **Nijhawan, Vishin** and **AAPA** to include moving data from a network layer into a physical memory page, wherein the network layer receives and transmits the data as data packets that are odd sized, arrive asynchronously, and contain metadata embedded with real data since references are all directed to virtual memory management systems to access data over a computing network, hence, would be considered to be analogous based on their related fields of endeavor.

One would be motivated to do so to extend the address space to memory outside the cluster by using virtual memory management system to manage access to remote physical address through the use of a remote page table and/or an auxiliary translation lookaside buffer (**Vishin, col. 1, lines 5-9 and lines 54-63**).

5. As to claim 2, **Nijhawan-Vishin-AAPA** teaches the method of claim 1, further comprising:

dividing the physical memory pages into physical memory clusters (*i.e., dividing the memory into memory block/pages 92 and 94 with size from 4K to 4M*) such that the data received by the network layer is stored into the physical memory clusters (*i.e., such that the data is stored in memory blocks/pages 92 and 94 as illustrated in Fig. 9*) (**Nijhawan, Fig. 9 and col. 10, lines 7-16**).

6. As to claim 3, **Nijhawan-Vishin-AAPA** teaches the method of claim 1, further comprising:

creating a plurality of logical pages based on the offset and length of the data associated with a network write operation (*i.e., if the page being mapped by 32-bit linear address 81 is a 8K page, then the upper 9 bits of the 10+12 bit offset can be used to define the page number such that a 19-bit logical page number is provided and a 13-bit offset is provided as an offset within the 8K page, wherein the logical page number is mapped or translated to a physical page number to access, i.e., to read and write data to the target physical memory/location*) (**Nijhawan, col. 4, lines 3-6 and col. 8, lines 40-51**).

7. As to claim 4, **Nijhawan-Vishin-AAPA** teaches the method of claim 1, further comprising:

creating a read only logical page comprising zeros, i.e., comprising uninitialized data (*i.e., the OS ensures that all memory blocks are aligned on a 4M linear address boundary so that the lower 22 bits of the starting linear address of the memory blocks are zero*) (**Nijhawan, col. 2, lines 1-5**).

8. As to claim 5, **Nijhawan-Vishin-AAPA** teaches the method of claim 1, further comprising:

merging an existing physical memory cluster with a new physical cluster based on the offset and length of the existing physical memory cluster and based on the offset and length of the new physical memory cluster (*i.e., within the allocated 128K of memory, the OS inherently maps a 64K block of memory that resides in physical memory on 64K boundaries, which can be used for the desired 40K block, and then the extra memory on either side of the 64K boundaries can be reallocated, i.e., remerged*) (**Nijhawan, col. 9, line 61 – col. 10, line 16**).

9. Claims 6-11 are corresponding system claims of method claims 1-5; therefore, they are rejected under the same rationale.

10. Claims 14-18 are corresponding computer-readable medium claims of method claims 1-5; therefore, they are rejected under the same rationale.

11. **Claims 19-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nijhawan-Vishin-AAPA, and further in view of Richter (US 2003/0097481 A1).**

12. As to claims 19-20, **Nijhawan-Vishin-AAPA** teaches the method of claim 1, wherein, as taught by **Vishin**, network clusters 102 transmits and receives the data as data packets over the computer network 114 via network interconnectivity such as network switches as illustrated in Fig. 9, but does not explicitly teach the network layer uses a transport control protocol / Internet protocol (TCP/IP) to transmit and receive the data as data packets over a computer network such as the Ethernet.

In an analogous art, **Richter** teaches a content delivery system that receives and transmits data packets, wherein the network interface engine (*i.e., the network layer*) performs the MAC, IP, TCP or UDP header identification, verification and checksum validation/generation, etc., in receiving and transmitting the data packets (**Richter, paragraph [0072]**).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to combine the teachings of **Nijhawan-Vishin-AAPA** and **Richter** to use TCP/IP to transmit and receive the data as data packets over the Ethernet network since references are all directed to network connected computing systems to transmit and receive data over a computing network, hence, would be considered to be analogous based on their related fields of endeavor.

One would be motivated to do so to allow the computing systems using the well-established networking protocol stack TCP-UDP/IP suite to verify end-to-end data integrity to ensure that intermediate forwarding nodes (*such as network switches on*

network 114 of Vishin), client memory problems, and statistically remote errors have not corrupted the original data packets in transmitting and receiving the data packets over the Ethernet network (**Richter, paragraph [0003]**).

13. Claims 23-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nijhawan-Vishin-AAPA, and further in view of Westbrook et al. (US 6,934,760), hereinafter "**Westbrook**".

14. As to claim 23, **Nijhawan-Vishin-AAPA** teaches the method of claim 1, but does not explicitly teach the data packets arrive in a sequence that is different from an original sequence in which they were transmitted.

In an analogous art, **Westbrook** teaches typically, packets of the original stream are marked with a sequence number, timestamp, or other ordering indication, and then dynamically routed and distributed among different paths and arriving at a location possibly out of their original sequence (*i.e., data packets arrive in a sequence that is different from an original sequence in which they were transmitted*) (**Westbrook, Abstract and col. 3, lines 40-45**).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to combine the teachings of **Nijhawan-Vishin-AAPA** and **Westbrook** to include the feature of data packets arriving in a sequence that is different from an original sequence. One would be motivated to do so to achieve high reliability and increased performance at a reasonable price by dynamically routing and distributing packets of information among multiple paths between a source and a

destination since it is more cost-effective and technical feasible to provide multiple slower rate links or switching paths than to provide a single higher rate path (**Westbrook, col. 1, lines 26-36**).

15. Claims 24-25 are corresponding system and article claims of method claim 23; therefore, they are rejected under the same rationale.

(10) Response to Argument

- Appellant argued (for claims 1, 2, 4, 6, 7, 9, 10, 14, 15 and 17) in substance that
(A) *“Appellant submits that Vishin’s network (referred hereinafter as “network 114”), as described in Fig. 1 and the passage at col. 1, lines 12-24, is simply a connection of multiple processor clusters that is neither disclosed nor suggested whatsoever to move data from a network layer into a physical memory page”, as argued in page 10 of the Appeal Brief.*

As to point (A), **Vishin** teaches a distributed computer system having a primary translation lookaside buffer for storing page table entries and translating virtual (*i.e., logical*) addresses into physical addresses governed by a memory controller 112 that can also send requests via a network 114 to pull in, *i.e., to access, pages of data stored in the memory stores or secondary memory of other clusters 102 or other devices coupled to the network 114 via network switches as illustrated in Figs. 1 and 9 (Vishin, Figs. 1 and 9, and col. 1, lines 12-24).*

Examiner respectfully submits that one of ordinary skill in the art would appreciate that in networks, network switches operate at the data link layer (layer 2) and sometimes at the network layer (layer 3) to filter and forward data packets between network segments (supported by "What is switch? - A Word Definition From the Webopedia Computer Dictionary", <http://www.webopedia.com/TERM/s/switch.html>"), hence, in order to support the data operations such as to move, access, or write data from/to a remote cluster 102 connected to the network 114 via network switches by pulling in pages of data stored in the memory stores or secondary memory of other clusters 102 or other devices coupled to the network 114 via network switches as illustrated in Figs. 1 and 9, it should include the step of moving data from a network layer into the memory stores, i.e., moving data from network layer into a physical memory.

Hence, Examiner respectfully submits "*Vishin's network (as "network 114") does support/include a network layer that routes data packets from a cluster 102 (i.e., with a source network address) to another cluster 102 (i.e., with a destination address).*"

(B) "*There is nothing in Vishin that discloses or suggests that Vishin's network 114 transmits and receives data as data packets. Although Vishin describes transmitting data over the network 114, Vishin is silent as to whether the data is transmitted as packets or in some other form, e.g., serial bits. Absent any disclosure in Vishin of the type of the network 114 or the format of data transmitted over the network 114, Vishin's network 114 cannot be construed to be a network that transmits and receives data as data packets*", as argued in page 11 of the Appeal Brief.

As to point (B), **Vishin** teaches a distributed computer system having a primary translation lookaside buffer for storing page table entries and translating virtual (*i.e., logical*) addresses into physical addresses governed by a memory controller 112 that can also send requests via a network 114 to pull in, *i.e., to access*, pages of data stored in the memory stores or secondary memory of other clusters 102 or other devices coupled to the network 114 via network switches as illustrated in Figs. 1 and 9 (**Vishin**, Figs. 1 and 9, and col. 1, lines 12-24).

Examiner respectfully submits that since network switches operate at the data link layer (layer 2) and sometimes at the network layer (layer 3) to filter and forward data packets between network segments (*as defined in "What is switch? - A Word Definition From the Webopedia Computer Dictionary", attached herein with the Examiner's Answer as a supportive reference*), therefore, in order to support the data operations such as to move, access, or write data from/to remote clusters 102 or other devices connected to the network 114 via network switches as illustrated in Figs. 1 and 9, it should include the step of transmitting and receiving data as data packets over the network 114 via network switches.

Hence, Examiner respectfully submits, "*Vishin's network (as "network 114")*" can be construed as a network that transmits and receives data as data packets, as claimed in the invention.

(C) "*There is nothing in Vishin that suggests that network 114 is anything more than a simple connection between processor clusters, which could, for example, be implemented by a serial connection that sends data one bit at a time, not as packets.*"

Thus, neither Nijhawan nor Vishin provide any suggestion as to why one skilled in the art would be motivated to modify their systems with AAPA to transmit and receive packets, and in particular, to transmit and receive data packets that are odd-sized, arrive asynchronously, and contain metadata embedded with real data”, as argued in page 13 of the Appeal Brief.

As to point (C), contrary to the Appellant's assertion, Vishin's network 114 **is not** a simple connection between processor clusters implemented by a serial connection that sends data one bit at a time, but a switching network that can filter and forward data packets between network segments as described in points (A) and (B) above.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to combine the teachings of **Nijhawan, Vishin and AAPA** to include moving data from a network layer into a physical memory page, wherein the network layer receives and transmits the data as data packets that are odd sized, arrive asynchronously, and contain metadata embedded with real data since references are all directed to virtual memory management systems to access data over a computing network, hence, would be considered to be analogous based on their related fields of endeavor.

One would be motivated to do so to extend the address space to memory outside the cluster by using virtual memory management system to manage access to remote physical address (via a switching network such as network 114 as illustrated in Fig. 9) through the use of a remote page table and/or an auxiliary translation lookaside buffer (**Vishin, col. 1, lines 5-9 and lines 54-63**).

Also, in response to applicant's argument that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988) and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992).

In this case, Examiner has clearly shown that the combined teachings of the cited references and AAPA have rendered each and every aspect of Appellant's claimed invention and would have been obvious to one having ordinary skill in the art, and as such Examiner has met his burden in rendering Appellant's claim invention (for claims 1, 2, 4, 6, 7, 9, 10, 14, 15 and 17) unpatentable.

- Appellant argued (for claims 3, 8 and 16) in substance that

(D) *"There is nothing in Nijhawan that discloses or suggests that a logical page number or an associated logic page is based on the offset and length of the data associated with a network write operation"*, as argued in page 14 of the Appeal Brief.

As to point (D), **Nijhawan** teaches if the page being mapped by 32-bit linear address 81 is a 8K page, then the upper 9 bits of the 10+12 bit offset can be used to define the page number such that a 19-bit logical page number is provided and a 13-bit offset is provided as an offset within the 8K page (*i.e., define/generate a logical page based on the offset and length of the data*), wherein the logical page number is mapped

or translated to a physical page number to access, i.e., to read and write data to the target physical memory/location (**Nijhawan**, col. 4, lines 3-6 and col. 8, lines 40-51).

Also, Examiner respectfully submits that Appellant acknowledges *"Nijhawan describes using the offset of an 8K page to generate a logical page number"* and *"in Nijhawan, a logical page can assist a network write operation with accessing data stored in a physical page that is mapped to the logical page"* (see page 14 of the Appeal Brief).

Hence, **Nijhawan** does teach or suggest, *"a logical page number or an associated logic page is based on the offset and length of the data associated with a network write operation"*, as argued in page 14 of the Appeal Brief.

- Appellant argued (for claims 5, 11 and 18) in substance that

(E) *"The Examiner incorrectly interprets the term "reallocated" as meaning the same as "remerged" or "merged", wherein the merging of an existing physical memory cluster with a new physical cluster involves combining the existing and new clusters such that they occupy either the same, overlapping, or contiguous segments of physical memory"*, as argued in page 15 of the Appeal Brief.

As to point (E), before addressing the argument, Examiner respectfully submits that in response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., *"the merging of an existing physical memory cluster with a new physical cluster involves combining the existing and new clusters such that they occupy either the same, overlapping, or contiguous segments of physical memory"*) are not recited in the

rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

In this case, **Nijhawan** teaches within the allocated 128K of memory, the OS inherently maps a 64K block of memory that resides in physical memory on 64K boundaries, which can be used for the desired 40K block, and then the extra memory on either side of the 64K boundaries can be reallocated (*hence, Nijhawan does teach combining the existing and new physical memory*) (**Nijhawan, col. 9, line 61 – col. 10, line 16**).

- Appellant argued (for claims 19 and 20) in substance that

(F) *“There is nothing in Richter that describes or suggests the use of translation lookaside buffer such as those disclosed in Nijhawan or Vishin. Furthermore, as discussed above, neither Nijhawan nor Vishin disclose or suggest anything that would motivate a person of ordinary skill in the art to modify their systems to transmit data over a network as data packets, a feature required by AAPA and Richter ... The Examiner’s proffered combination of Nijhawan, Vishin, AAPA, and Richter amounts to a hindsight combination, which is improper as a matter of law”, as argued in page 17 of the Appeal Brief.*

As to point (F), first, in response to applicant's arguments against the references individually *“There is nothing in Richter that describes or suggests the use of translation lookaside buffer such as those disclosed in Nijhawan or Vishin”, one cannot show nonobviousness by attacking references individually where the rejections are based on*

combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

Second, in response to applicant's arguments that "*neither Nijhawan nor Vishin disclose or suggest anything that would motivate a person of ordinary skill in the art to modify their systems to transmit data over a network as data packets, a feature required by AAPA and Richter*", Examiner respectfully submits that **Vishin** does teach the network 114 is a switching network as illustrated in Fig. 9, that uses network switches to filter and forward/transmit data between network clusters 102 across the network 114 as data packets (**Vishin, Figs. 1 and 9, and col. 1, lines 12-24**). Hence, **Vishin** does teach a system that receives and transmits data over a network as data packets, a feature required by **AAPA** and **Richter**.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to combine the teachings of **Nijhawan-Vishin-AAPA** and **Richter** to use TCP/IP to transmit and receive the data as data packets over the Ethernet network since references are all directed to network connected computing systems to transmit and receive data over a computing network, hence, would be considered to be analogous based on their related fields of endeavor.

One would be motivated to do so to allow the computing systems using the well-established networking protocol stack TCP-UDP/IP suite to verify end-to-end data integrity to ensure that intermediate forwarding nodes (*such as network switches on network 114 of Vishin*), client memory problems, and statistically remote errors have not corrupted the original data packets in transmitting and receiving the data packets over the Ethernet network (**Richter, paragraph [0003]**).

Third, in response to applicant's argument that the examiner's conclusion of obviousness is based upon improper hindsight reasoning, it must be recognized that any judgment on obviousness is in a sense necessarily a reconstruction based upon hindsight reasoning. But so long as it takes into account only knowledge which was within the level of ordinary skill at the time the claimed invention was made, and does not include knowledge gleaned only from the applicant's disclosure, such a reconstruction is proper. See *In re McLaughlin*, 443 F.2d 1392, 170 USPQ 209 (CCPA 1971).

- Appellant argued (for claims 23-25) in substance that

(G) *"There is nothing in Westbrook that describes or suggests the use of translation lookaside buffer such as those disclosed in Nijhawan or Vishin. Furthermore, as discussed above, neither Nijhawan nor Vishin disclose or suggest anything that would motivate a person of ordinary skill in the art to modify their systems to transmit data over a network as data packets, a feature required by AAPA and Westbrook", as argued in page 18 of the Appeal Brief.*

As to point (G), first, in response to applicant's arguments against the references individually *"There is nothing in Westbrook that describes or suggests the use of translation lookaside buffer such as those disclosed in Nijhawan or Vishin", one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references.* See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

Second, in response to applicant's arguments that *"neither Nijhawan nor Vishin disclose or suggest anything that would motivate a person of ordinary skill in the art to modify their systems to transmit data over a network as data packets, a feature required by AAPA and Westbrook"*, Examiner respectfully submits that **Vishin** does teach the network 114 is a switching network as illustrated in Fig. 9, that uses network switches to filter and forward/transmit data between network clusters 102 across the network 114 as data packets (**Vishin, Figs. 1 and 9, and col. 1, lines 12-24**). Hence, **Vishin** does teach a system that receives and transmits data over a network as data packets, a feature required by **AAPA** and **Westbrook**.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to combine the teachings of **Nijhawan-Vishin-AAPA** and **Westbrook** to include the feature of data packets arriving in a sequence that is different from an original sequence. One would be motivated to do so to achieve high reliability and increased performance at a reasonable price by dynamically routing and distributing packets of information among multiple paths between a source and a destination since it is more cost-effective and technical feasible to provide multiple slower rate links or switching paths than to provide a single higher rate path (**Westbrook, col. 1, lines 26-36**).

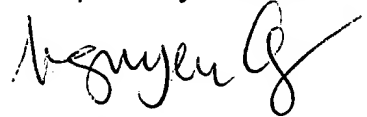
(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

Art Unit: 2141

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,



Quang N. Nguyen

Conferees:



Lynne H. Browne
Appeal Specialist, TQAS
Technology Center 2100



RURAL DHARIA
SUPERVISORY PATENT EXAMINER

Fish & Richardson P.C.
225 Franklin Street
Boston, MA 02110
Telephone: (617) 542-5070
Facsimile: (617) 542-8906



Find out how Microsoft works with global partners to help make computing safer ➔

Your potential. Our
Microsoft

internet.com

You are in the: Small Business Computing Channel

View
Sites +

Small Business
Computing Channel

Generate Complete .NET Web Apps in Minutes . Download Iron Speed Designer today.

internet.com

(Webopedia)

The #1 online encyclopedia
dedicated to computer technology

Enter a word for a definition...

...or choose a computer category.

MENU

[Home](#)
[Term of the Day](#)
[New Terms](#)
[Pronunciation](#)
[New Links](#)
[Quick Reference](#)
[Did You Know?](#)
[Categories](#)
[Tech Support](#)
[Webopedia Jobs](#)
[About Us](#)
[Link to Us](#)
[Advertising](#)

Compare Prices:

HardwareCentral

Talk To Us...

[Submit a URL](#)
[Suggest a Term](#)
[Report an Error](#)

GET FREELANCER.com

Need Custom Work

switch

(switch) (n.) (1) In networks, a device that filters and forwards packets between LAN segments. Switches operate at the data link layer (layer 2) and sometimes the network layer (layer 3) of the OSI Reference Model and therefore support any packet protocol. LANs that use switches to join segments are called switched LANs or, in the case of Ethernet networks, switched Ethernet LANs.

(2) A small lever or button. The switches on the back of printers and on expansion boards are called DIP switches. A switch that has just two positions is called a toggle

Last modified: Monday, November 13, 2006

Powerful mobile computer,
meet powerful backup.

The HP Compaq nx9420
Business Notebook with
Intel® Centrino® Duo Mobile
Technology.

[Learn more >](#)



Dual-core.
Do more.

THE
COMPUTER
IS PERSONAL
AGAIN.



**FIND THE RIGHT IBM RATIONAL
TOOLS FOR YOUR PROJECT**

Rational Application Developer

Powered by Eclipse, optimized for IBM WebSphere software, supports multi-vendor runtime environments. Quickly design, develop, analyze, test, profile and deploy high-quality Web, service-oriented architecture (SOA), Java, J2EE, and portal applications. RAD includes basic UML diagram support and utilizes class and sequence diagrams as they apply to code visualization and visual editing of code.

Rational Software Architect

Includes all of the J2EE, Web, and Web services features of Rational Application Developer for WebSphere but delivers a more complete and robust model-driven development experience. Leverages model-

internet.com

[Developer](#)
[International](#)
[Internet Lists](#)
[Internet News](#)
[Internet Resources](#)
[IT](#)
[Linux/Open Source](#)
[Personal Technology](#)
[Small Business](#)
[Windows Technology](#)
[xSP Resources](#)
[Search internet.com](#)
[Advertise](#)
[Corporate Info](#)
[Newsletters](#)
[Tech Jobs](#)
[E-mail Offers](#)

internet commerce

[Be a Commerce Partner](#)
[Promotional](#)
[Education Degrees](#)
[CRM Software](#)
[Cheap Plane Tickets](#)
[Corporate Gifts](#)
[Business Web Hosting](#)
[Digital Camera Memory](#)
[Website Templates](#)
[Economy Server Racks](#)
[2nd Mortgage](#)
[IT Jobs](#)
[Promotional Items](#)
[2007 New Cars](#)
[Merchant Accounts](#)

switch.

(3) Another word for option or parameter -- a symbol that you add to a command to modify the command's behavior.

driven development with the UML for creating well-architected applications and services

Rational Software Modeler

A customizable, UML-based visual modeling and design tool that enables users to clearly document and communicate these system views. Its drag and drop UI components and point and click database connectivity leverages your existing skills, shortens the Java learning curve, and supports team development.

Rational Systems Developer

IBM Rational Systems Developer is a design and development tool that enables software architects and model-driven developers to create well-architected C/C++, Java J2SE, and CORBA-based applications that leverage Unified Modeling Language (UML 2).

[Click here to learn more.](#)

•E-mail this definition to a colleague•**Sponsored listings**

Digi-Key: E-Switch Switch - Broad-line distributor web site features real-time stock status and pricing, online ordering, RFQ, technical support, product datasheets and photos.

Citrix Application Gateway: IP Telephony Application Access - Access that is secure and simple for users and adaptable to almost any access situation.

Quintum Technologies, Inc.: VoIP Telephony Solutions - Offers Voice over IP (VOIP) products and systems, including service provider solutions, and enterprise solutions.

For internet.com pages about **switch**
CLICK HERE. Also check out the following links!

LINKS

🚀 = Great Page!

Network Switching Tutorial 🚀

How can you tell if your network will benefit from switching? And how do you add switches to your network design for the most benefit? This tutorial is written to answer these questions.

Open Networks Today 🚀

Networking news moves at a fast pace, and Open Networks Today lets you keep up with it. Open Networks Today offers its readers the ability to control how news is presented through customizing content filters, discussions, and news feed links.

PracticallyNetworked.com 🚀

PracticallyNetworked.com provides easy-to-

Related Categories

[Business Computing](#)

[Hardware](#)

[Networking Hardware](#)

Related Terms

[3COM](#)

[backpressure](#)

[BPDU](#)

[DIP switch](#)

[hub](#)

[option](#)

[parameter](#)

[router](#)

[routing switch](#)

[switched Ethernet](#)

[toggle](#)

(Webopedia)

Give Us Your
Feedback

Networking Hubs and
Switches
switch Products

understand help for small-network builders. The site contains how-to information for setting up and debugging home-office and small-business networks. Users can also find extensive troubleshooting information, tips on getting applications to work through firewalls, product reviews on network hardware and software, and more.

PracticallyNetworked.com Discussion Forums ➤

If network connections, sharing computers, router problems or other networking issues are bogging you down, then the PracticallyNetworked.com discussion forum is the place to be. Here you'll find help and support for all your network-related problems.

What's the Difference Between Routers, Switches and Hubs? ➤

Many people use the terms routers, switches and hubs interchangeably. However, the functions of the three devices are all quite different from one another, even if at times they are all integrated into a single device.

Switch Buyer's Directory

LAN Times site with information finding the right switches for your needs and budget. The directory features switches in nearly all categories: ATM, ethernet, Fast Ethernet, Gigabit Ethernet, FDDI, and token ring.

Sponsored listings

Siemens Industrial Automation: Electrical Switches - PROFINET offers decentralized IO, peer-to-peer communications, data visibility, machine safety, and motion control on one Industrial Ethernet network.

GlobalSpec.com: Electrical Level Switches - Provides database of suppliers for Electrical Level Switches. Browse catalogs and view technical information.

QVS: Computer Switch Boxes - Manufactures cables and connectivity products for the computer and communication industries. Parallel, SCSI, Mac, KVM, ethernet, and USB switches.

Switch Boots: Lamb Industries - Manufacturer of industrial switches including toggle switches, rocker switches, pressure switches, pushbutton switches, slide switches and more.

GlobalSpec.com: Industrial Switch Magnets - Provides database of suppliers for Industrial Switch Magnets. Browse catalogs and view technical information.

Shop by Top Models:
Cisco Catalyst® 2950-24
24-Port Ethernet Switch
(WS-C2950-24)
 18 store offers from \$395 - \$700

Cisco Catalyst 3560 24-
Port Ethernet Switch (ws-
c3560-24ps-s)
 20 store offers from \$1 - \$2883

Linksys EtherFast
EZXS55W 5-Port Ethernet
Switch
 20 store offers from \$20 - \$40

Cisco Catalyst 2960-24TT
24-Port Ethernet Switch
(WSC296024TTL)
 16 store offers from \$703 - \$1035

EZ SMC8508T 8-Port
Gigabit Ethernet Switch
 15 store offers from \$56 - \$120